University of Twente
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CλasH

From Haskell To Hardware

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September 3, 2009

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http://caes.ewi.utwente.nl

What will we see?

- Small tour: what can we describe in CλasH
- Quick real demo

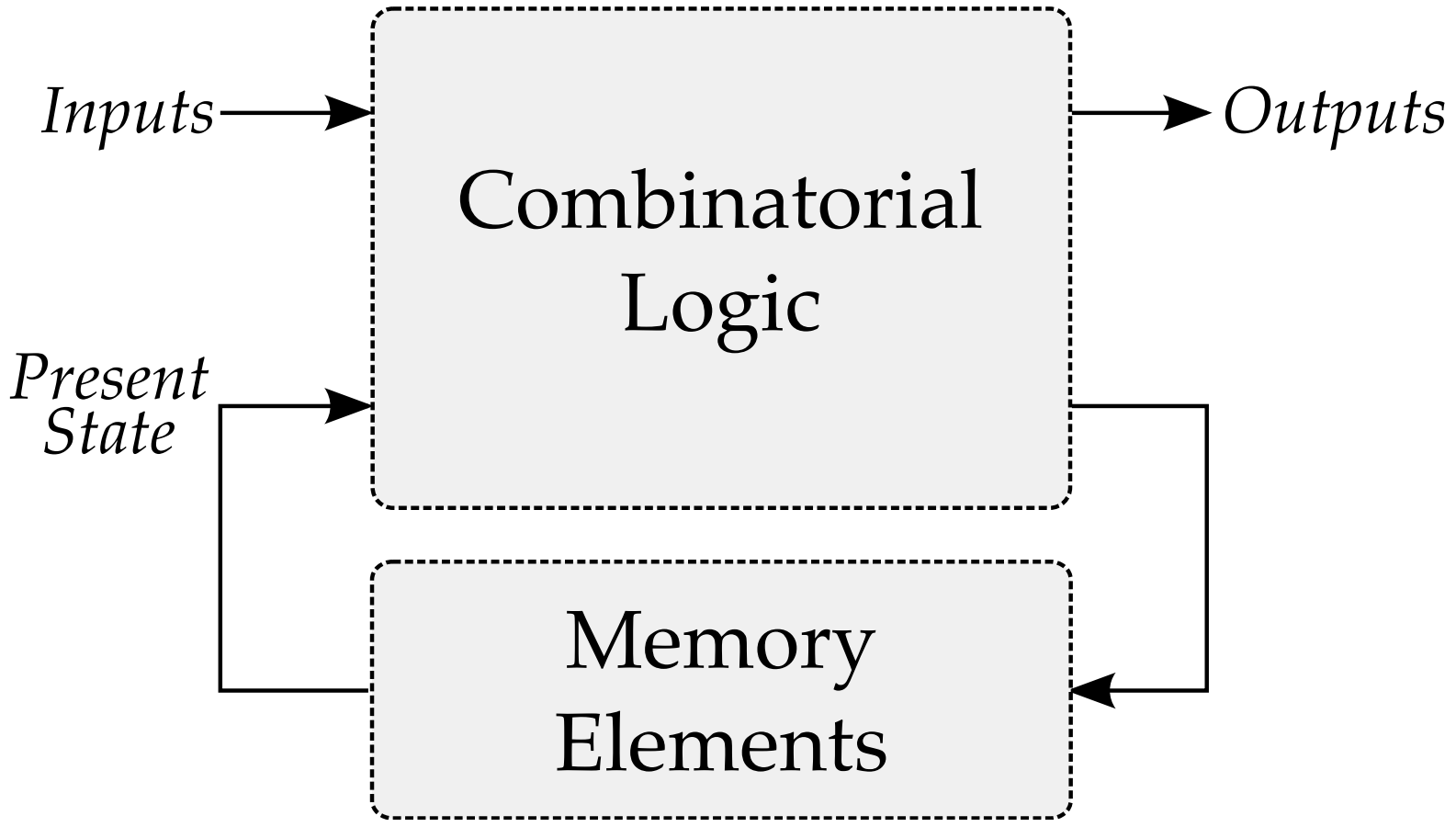
Virtuele demo

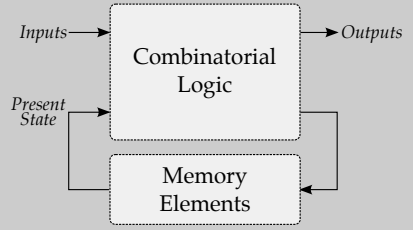
What is CλasH?

- CλasH: CAES Language for Hardware Descriptions
- Rapid prototyping language
- Subset of Haskell can be translated to Hardware (VHDL)
- Structural Description of a Mealy Machine

- Wij zijn wij
- CλasH voor rapid prototyping
- Subset haskell vertaalbaar
- Mealy machine beschrijving

Mealy Machine





Voor wie het niet meer weet, dit is een mealy machine

Haskell Description

```
mealyMachine ::
  InputSignals →
  State →
  (State, OutputSignals)
mealyMachine inputs state = (new_state, output)
  where
    new_state = logic state input
    outputs = logic state input
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Simulating a Mealy Machine

$$
\begin{aligned}
&\mathit{run}\ \mathit{func}\ \mathit{state}\ [\,] = [\,] \\
&\mathit{run}\ \mathit{func}\ \mathit{state}\ (i : \mathit{input}) = o : \mathit{out} \\
&\quad \textbf{where} \\
&\qquad (\mathit{state}', o) = \mathit{func}\ \mathit{state}\ i \\
&\qquad \mathit{out} = \mathit{run}\ \mathit{func}\ \mathit{state}'\ \mathit{input}
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Small Use Case

- Small Polymorphic, Higher-Order CPU
- Each function is turned into a hardware component
- Use of state will be simple

Imports

Import all the built-in types, such as vectors and integers:

import *CLasH.HardwareTypes*

Import annotations, helps CλasH to find top-level component:

import *CLasH.Translator.Annotations*

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First we define some ALU types:

$$\textbf{type } Op\ s\ a\ = a \rightarrow Vector\ s\ a \rightarrow a$$
$$\textbf{type } Opcode = Bit$$

And some Register types:

$$\textbf{type } RegBank\ s\ a = Vector\ (s + D1)\ a$$
$$\textbf{type } RegState\ s\ a = State\ (RegBank\ s\ a)$$

And a simple Word type:

$$\textbf{type } Word = SizedInt\ D12$$

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We make a primitive operation:

$$primOp :: (a \rightarrow a \rightarrow a) \rightarrow Op\ s\ a$$
$$primOp\ f\ a\ b = a\ `f`\ a$$

We make a vector operation:

$$vectOp :: (a \rightarrow a \rightarrow a) \rightarrow Op\ s\ a$$
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We define a polymorphic ALU:

```
alu ::
    Op s a →
    Op s a →
    Opcode → a → Vector s a → a
alu op1 op2 Low  a b = op1 a b
alu op1 op2 High a b = op2 a b
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We define a polymorphic ALU:

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Make a simple register bank:

```
registerBank ::
  (Some context...) =>
  (RegState s a) -> a -> RangedWord s ->
  RangedWord s -> Bit -> ((RegState s a), a)
registerBank (State mem) data_in rdaddr wraddr wrenable =
  ((State mem'), data_out)
  where
    data_out = mem ! rdaddr
    mem' | wrenable == Low = mem
         | otherwise       = replace mem wraddr data_in
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Combining ALU and register bank:

```
{-#ANN actual_cpu TopEntity#-}
actual_cpu ::
  (Opcode, Word, Vector D4 Word, RangedWord D9,
  RangedWord D9, Bit) → RegState D9 Word →
  (RegState D9 Word, Word)
actual_cpu (opc, a, b, rdaddr, wraddr, wren) ram =
  (ram', alu_out)
  where
    alu_out = alu simpleOp vectorOp opc ram_out b
    (ram', ram_out) = registerBank ram a rdaddr wraddr wren
    simpleOp = primOp (+)
    vectorOp = vectOp (+)
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Is CλasH usable?

- It can be used for more than toy examples
- We designed a matrix reduction circuit
- We simulated it in Haskell
- Simulation results in VHDL match
- Synthesis completes without errors or warnings

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So how do you make Hardware from Haskell?

In three simple steps

- No Effort:
  GHC API Parses, Typechecks and Desugars Haskell
- Hard.. sort of:
  Transform resulting Core, GHC's Intermediate Language, to a normal form
- Easy:
  Translate Normalized Core to synthesizable VHDL

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How do we use CλasH?

As a library:

- Import the module: CLasH.Translator
- And call *makeVHDLAnnotations ghc_lib_dir [files_to_translate]*

Customized GHC:

- Call GHC with the –vhdl flag
- Use the :vhdl command in GHCi

Real Demo

- We will simulate the small CPU from earlier
- Translate the CPU code to VHDL
- Simulate the generated VHDL
- Synthesize the VHDL to get a hardware schematic

Some final words

- Still a lot to do: make a bigger subset of Haskell translatable
- Real world designs work
- We bring functional expressivity to hardware designs

Thank you for listening